Amendments to the Specification:

Please replace the paragraph on page 8, lines 23-33 with the following new paragraph:

Further understanding of operation of the device of FIG. 3A is provided through FIG. 5. FIG. 5 illustrates one embodiment of the physical layout of the switch matrix. The switch matrix includes a first and a second element. The first element E1 includes a semiconductor substrate SL1 with a plurality of active elements AL1-ALN (with a first active element AL1 shown in FIG. 5) fabricated on and spaced throughout the substrate. A plurality of programmable registers PL1-PLN (with a first programmable register PL1 shown in FIG. 5) corresponding to the plurality of active elements are also included on the semiconductor substrate. Each of the plurality of programmable registers are commonly coupled and controlled by a programming interface (not shown).

Please replace the paragraph on page 8, starting on line 34 and continuing to page 9, ending at line 11 with the following new paragraph:

The second element E2 includes a first layer of a first set of conducting transmission lines and a second layer of a second set of conducting transmission lines. The second set of conducting transmission lines are arranged to be orthogonal to the first set of conducting transmission lines. The first and second set of conducting transmission lines are separated by an

insulating layer IL1. In one embodiment, the first and second set of conducting transmission lines are fabricated from a laminate of insulating material between a conducting layer having a pattern forming an array of multiple parallel controlled-impedance transmission lines. The placement of the active elements in the first elements is arranged to align with the intersections of the first set of conducting transmission lines with the second set of conducting transmission lines. Inputs to the switch matrix are provided at a first layer for the first set of conducting transmission lines. Similarly, outputs from the switch matrix are provided at a second layer for the second set of conducting transmission lines.

Please replace the paragraph on page 20, lines 4-22 with the following new paragraph:

As noted above, in reference to FIG. 1, the switch includes a primary access port coupled to the programming interface. In the event that the primary access port is busy or otherwise occupied, in one embodiment, the switch includes a secondary access port 113. The secondary access port is coupled to the programming interface and is configured to communicate with the programming interface independent of the primary access port. In particular, the secondary access port allows asynchronous "readback" of connection states of the switch matrix module, while the primary access port is actively programming the switch. Readback refers to retrieving, i.e., reading back, current pending information from a register coupled to the switch matrix module. For example, the programming information

in the staging registers or the user registers are retrieved by activating the readback control. The secondary access port also allows configuration control of the switch matrix module, such as control operation of the DRIVE and SENSE connections, input equalization, output drive level control, boundary scan operations, temperature sensing and pseudo-random binary sequence (PRBS) functions.